On Chip Tap Delay Measurements For A Digital Delay Line

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On Chip Tap Delay Measurements

On-Chip Tap-Delay Measurements for a Digital Delay-Line Used in High-Speed Inter-Chip Data Communications. Conference Paper (PDF

Available) in Proceedings of the Asian Test Symposium · January ...

(PDF) On-Chip Tap-Delay Measurements for a Digital Delay ...

On-chip tap-delay measurements for a digital delay-line used in high-speed inter-chip data communications Abstract: During the last few years, new synchronization techniques to send data between ICs at increasingly high data-rates have been developed. Some of them rely on digital delay lines.

On-chip tap-delay measurements for a digital

delay-line ...

On-Chip Tap-Delay Measurements for a Digital Delay-Line Used in High-Speed Inter-Chip Data Communications. Share on. Authors: Octavian Petre. View Profile, Hans G. Kerkhoff. View Profile. Authors Info & Affiliations ; Publication: ATS '02: Proceedings of the 11th Asian Test Symposium November 2002 .

On-Chip Tap-Delay Measurements for a Digital Delay-Line ...

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chip, in which there are two rows of PDEs and their numbers are

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Petre, O., & Kerkhoff, H. G. (2002). On-Chip Tap Delay Measurements for a Digital Delay Line Used in High-Speed Inter-Chip Data Communications.In Proceedings of the Eleventh Asian Test Symposium (pp. 122-127).Guam, USA.

On-Chip Tap Delay Measurements for a Digital Delay Line ...

On Chip Tap Delay Measurements For A Digital

Delay Line Author: ï¿½ï¿½www.logisticsweek.com-2020-08-30T00:00:00+00:01 Subject: ï¿½ï¿½On Chip Tap Delay Measurements For A Digital Delay Line Keywords: on, chip, tap, delay, measurements, for, a, digital, delay, line Created Date: 8/30/2020 3:26:59 PM

On Chip Tap Delay Measurements For A Digital Delay Line

On-Chip Tap-Delay Measurements for a Digital Delay-Line Used in High-Speed Inter-Chip Data Communications Octavian Petre, Hans G. Kerkhoff MESA+ Research Institute

On-Chip Tap-Delay Measurements for a Digital Delay-Line ...

On-Chip Tap Delay Measurements for a Digital Delay Line Used in High-Speed Inter-Chip Data Communications: Published in: Proceedings of the Eleventh Asian Test Symposium, 122 - 127: Author: Petre, O., Kerkhoff, Hans G. Date issued: 2002-11-18: Access: Restricted Access: Reference(s) METIS-208789: Language: und: Type: Conference Paper: Publication

On-Chip Tap Delay Measurements for a Digital Delay Line ...

In the design, the frequency of the reference

clock must be 310 MHz to guarantee that the tap delay of each PDE is suited to the measurement system. Then the tap delay is t tap= 1/(310 MHz×64)=50.4(ps). The system is implemented in a Xilinx FPGA chip, in which there are two rows of PDEs and their numbers are X0Y0-X0Y239 and X2Y0-X2Y239.

High-resolution short time interval measurement system ...

The timing accuracy of the delay lines is crucial for a good functionality of the synchronization mech-anism. This paper will present a strategy to measure the tap-delays

of a digital delay-line, using the well-known os-cillation technique. The occurring measurement error for the presented technique has been calculated.

CiteSeerX — On-Chip Tap-Delay Measurements for a Digital ...

O. Petre and H.G. Kerkhoff, “On-Chip Tap-Delay Measurements for a Digital Delay-Line Used in High-Speed Inter-Chip Data Communications,” in Asian Test Symposium, pp. 122-127, 2002. Google Scholar

On-Chip Random Jitter Testing Using Low Tap-

Count Coarse ...

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On Chip Delay Measurement : The Transition or

Delay faults are analyzed/debugged using On Chip Delay Measurement techniques. If these checks do not pass at the functional frequency, then the chip may not work as expected for a particular specifications. Note that these checks are performed before manufacturing of the chip.

What is the difference or what is meant by on-chip and off ...

Some on-chip path delay time measurement methods using embedded delay measurement were proposed [14]–[19]. In these, delay times of paths are measured. A modified vernier delay

line (VDL) method for path delay measurement also has been proposed [14]. This delay measurement method can achieve a high-precision capability.

Small Delay Testing Using On-chip Delay Measurement

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Delay Line

Tap Increment 3ps 5ps 10ps 11ps 15.7ps 20ps 50ps 150ps 250ps 500ps 1ns 2ns 2.5ns 3ns 4ns 5ns 6ns 7ns 7.5ns 8ns 9ns 10ns 12ns 12.5ns 15ns 17.5ns 20ns 25ns 30ns 35ns 40ns 40.2ns 45ns 50ns 60ns 60.2ns 70ns 80ns 90ns 100ns. ps ns.

Clock/Timing - Delay Lines | Integrated Circuits (ICs ...

AB - We report on implementation of random sampling methodology for on-chip measurements of the pin-to-pin propagation delay of single standard cells of core library. A test chip

has been implemented in 0.13m GL130SB (130nm Logic Process) technology at Dongbu HiTek and used to monitor up to picosecond's timing behavior of 32 DUT's of core library.

On-chip measurements of standard-cell propagation delay ...

$310 - A retro tape echo style delay with 4 heads, each with its own mix/feedback control. Features controls for delay time (40ms up to 1200ms), echo feedback, mood and tone of the repeats, rate and depth for sine wave modulation. Tap tempo/hold footswitch adds. Mono or stereo ping pong output

operation.

Best Tape Delay Pedals And Tape Echos In 2020 - A Shopping ...

multi-tap delay lines are used in the design of the interpolator then the value of the single segment delay ? and its standard deviation determines the precision of the time-interval (?tm) measurement. If the interpolator consists of n delay lines of relatively high resolution, then during a